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Carbon Nano Tube Field Effect Transistor based BBL-PTL full adders with level restorer structures

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Full Adder (FA) is an important component not only in arithmetic circuits, but also in designing and development in all types of processors. The performance parameter of the one bit full adder has been implemented to increase the speed of the system. In this paper two Carbon Nano Tube Field Effect Transistor (CNTFET) based level restorers are introduced to the sum circuit of the branch-based logic and pass transistor (BBL-PT) full adder. The proposed level restorers eliminate the existence of voltage step which is presented in the conventional full adder [1]. T.V.Rao *et. al* proposed level restorer circuits that have used +1.2 V supply rail voltage [2]. By using these level restorers we could able to achieve good delay performance. The proposed 1-BIT full adder is graded high as it has less power consumption with the conventional 1-BIT full adders. The performance of the proposed CNTFET based BBL-PT FA with new level restorer structures are examined using Cadence with 32 nm CNTFET technology files with a supply rail voltage of +0.8 V.

Keywords: CNTFET; Branch-based logic; Pass transistor logic.

1. INTRODUCTION

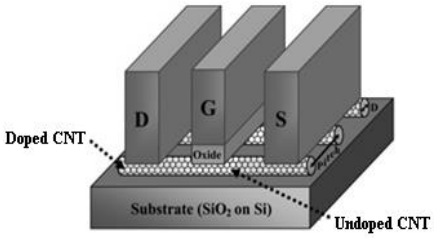
Adders are supposed to be an important components in each and every processor architecture. Generally, intensive research has been carried out to implement adders in different architectures, configurations, layouts, design styles and design methodologies. All these are implemented with the main purpose of improving adder speed and energy efficiency. Its speed mainly depends upon the delay, power consumption and power delay product. There also exist some conventional full adder structures and one amongst them is CMOS logic with 28 transistors and the other is PTL logic with 26 transistors. From this there arises large input capacitance but it cannot provide high speed operation. Another FA is Complimentary Pass Transistor Logic (CPL) with 32 transistors, but due to possessing a large number of internal

nodes and static inverters, it consumes a lot of power while it acquires high speed and full swing design [1-6].

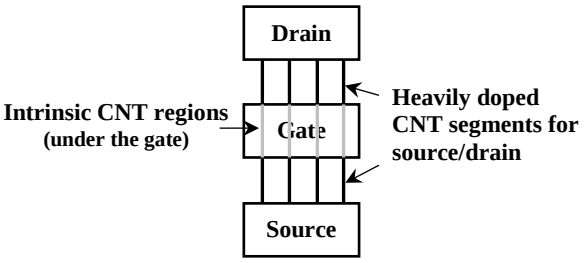
In this paper Pass Transistor Logic (PTL) is used to sum and branch based logic (BBL) to carry. There are many advantages in using this logic. It has simpler characterization and no diffusion interruption; moreover, it has a common drain for two branches with less number of contacts. The style in this design is mostly used to decrease parasitic capacitances [7-9]. From this, it achieves low power and also advantageous to acquire high speed. The major disadvantage is the voltage step that exists [1] to correct it; we can also use level restorers for the same purpose. In this paper this logic is implemented by using CNTFETs because of their advantages. It has more benefits while compared to the traditional MOSFET silicon based structure. CNTFETs have better control over channel formation. It has high electron mobility, high electron density and high transconductance when compared to traditional MOSFETs. Moreover, its threshold voltage and sub threshold slope is better than traditional MOSFETs [10-19].

Carbon Nano Tube (CNT) has gained popularity in the past few years for its tiny dimensions, special morphologies and also its potential implementing application in many emerging technologies. One of the examples of emerging technologies is cutting edge with in nanotechnology. It is capable of high efficiency and used in a wide range of applications in many streams of science and technology. CNTFETs consumes less power and proves much faster than the existing silicon based FETs [20].

A tube shaped material is a carbon nano-tube which is fabricated from carbon. By using the nanometer scale its diameter can be measured. These are fabricated from the graphite layer. Then the graphite sheet forms into a rolled up continuous, unbroken hexagonal mesh. These are the members of the fullerene family. These are long and hollow structures which appear to be containing one atom thick sheet of carbon called graphene [21]. Fig. 1(a) presents the schematic of cross sectional view and Fig. 1(b) top view CNTFET [22], [23].



(a) Cross sectional view



(b) Top view

Figure. 1: Schematic diagram of CNFET device.

CNTFETs are the next alternatives to the MOSFETs. These are said to be the molecular devices which prevent the fundamental silicon restriction in the ballistic transport. One of the CNTFET feature is their geometry that depends on threshold voltage. CNTFETS provides more advantages rather than silicon based technologies [24], [25].

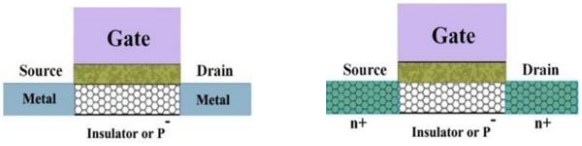
These are four terminal devices comprising of a nano-tubes acting as conducting channel, linking the source and drain contacts. According to the operation CNTFETs can be divided into two categories. They are Schottky Barrier CNTFET (SB-CNTFET) shown in Fig 2.(a) and MOSFET-like FET shown in Fig 2.(b) [26-30]. The conductivity of the Schottky Barrier CNTFET is regulated through the majority carriers tunneling over the Schottky barriers on the terminal contacts. The SB-CNFET on-current is achieved through the contact resistance. The Schottky Barriers placed at source/drain contacts are owing to the Fermi-level positioning of the metal and semiconductor interface. The height plus width of the Schottky Barriers, and consequently the conductivity, are tuned by the gate electrostatically. SB-CNFET presents the ambipolar conveying style. MOSFET like CNFET, exhibits the unipolar behavior by concealing either electron (p-CNTFET) or hole (n-CNTFET) transport with extrinsic source and drain.

The threshold voltage of a CNTFET is gauged by (1)

$$V_{th} \approx E_{bg} / 2\,e \approx 0.436 / D_{CNT}\,(nm) \tag{1}$$

where E_{bg} is the energy band gap of carbon nano-tube, e is the charge of electron, D_{CNT} is the carbon nano-tube diameter and n and m are the chirality of the CNT. It can be seen from (1) that the threshold voltage of a CNTFET is inversely related to the diameter of its nano-tubes, which is computed by (2)

$$D_{CNT} = d = 0.0783\sqrt{m^2 + n^2 + mn} \tag{2}$$



(a) (b)

Figure. 2: (a) SB-CNFET (b) MOS-CNFET

CNTFETs operating principle and device structure is similar to CMOS. Although CNTFETs have proved experimentally that they have excellent current capabilities. At 32 nm feature size it has been proved that at a single device level its presence effects the related process. CNTFETs have a different band structure which causes ballistic operation. So, there is a possibility of acquiring when compared to other nanotechnologies. So, it might be the reason that it has been used in high frequency and low voltage application devices. In CNFETS they have been classified into p-FET and n-FET devices and these devices are of the same size and have the same mobility. The current driving capability of transistor in sizing of complex circuits is also the same. To turn ON a CNTFET device, it requires a minimum threshold voltage and this voltage can be adjusted by changing the chiralities of CNT's. It makes the device more flexible when compared to the MOSFET. To achieve the required performance, it has to be operated under low voltage [31-41].

The remaining section of this paper is arranged as follows. Firstly, the proposed adders structure followed by its implementation and then its simulated results, finally it has ended up in conclusion.

2. Proposed circuits and operation

A full adder is a combination of its 3-inputs. The relation between the input and output can be expressed as

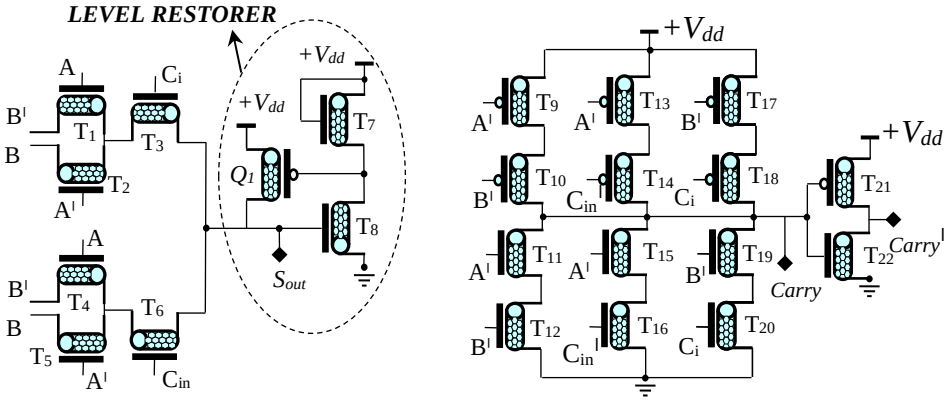
$$\text{Sum} = ABC_{in} + \overline{A}\overline{B}C_{in} + \overline{A}B\overline{C_{in}} + A\overline{B}\overline{C_{in}} \quad (3)$$

$$\text{Carry} = A.B + B.C_{in} + A.C_{in} \quad (4)$$

In this circuit by using minimum number of transistors and their intra connections; we can attain the low power consumption. Using the unsophisticated characterization makes the circuit very advantageous. This can be achived by branch based logic. It has many utilities that can be considered. It overcomes the diffusion capacitance that occurs in the circuit. So, by stepping in its foot prints it is found more advantageous in attaining low power and high speed.

2.1. CNTFET based proposed full-adder structure-I

The main disadvantage in this full adder is that it gives the weak output in the pass transistors. This cannot be accomplished by giving feedback to pull up as p-CNTFET transistor to sum block. To overcome this situation, it has to be made to supply sufficient drive in its subsequent stages. When a voltage step exists in the output node by 0 → 1 transition it can be used. This voltage drop and the delay that occurred in the level restores can be used to renew the weak logic '1' level. For the effected voltage step ON and OFF timings might not be equal. So to overcome this, the proposed adder should contain level restorers.



(a) (b)

Figure. 3: CNTFET based full adder with level restorer structure-I (within the dashed circle).

Here, in the circuit shown in Fig 3(a), it posses' n-CNTFET transistors from T_1 to T_6. While coming to the level restorer circuit, T_7 CNTFET where its gate is connected to the supply. For this n-channel transistor is always in ON condition. There exists only a p-CNTFET

(Q_1) which acts as a pull up for the network. So this type of methodology gives us high voltage gain.

When the voltage at node "S_{out}" is < $V_{dd}/2$, the n-CNTFETs (T_8) in the restorer will not reach switching threshold and therefore turned OFF. The resultant output of T_7 and T_8 CNTFETs is logic '1'. This logic '1' is the input to the pull-up p-CNTFETs (Q_1) and then pull-up Q_1 is turned OFF. The node "S_{out}" is charged with an effective drive current that equals the current of the n-CNTFETs network.

When the voltage at node "S_{out}" reaches to $V_{dd}/2$, the n-CNTFETs (T_8) in the restorer is turned ON. Then, the p-CNTFETs (Q_1) is turned ON and the effective drive current charging the capacitance at node "S_{out}" becomes the sum of the current flowing through the n-CNTFETs network and the pull-up p-CNTFETs (Q_1) currents.

2.2. CNTFET based proposed full-adder sum structure-II

In the second proposed CNTFET full adder sum circuit is shown in Fig. 4 and the carry circuit is shown in Fig. 3(b). When logic '1' is applied to the input of n-CNTFET network T_1 to T_6 shown in Fig. 2, then the logic '1' is passed through the n-CNTFET network, the node "S_{out}" is to be charged to a weak logic '1'. When the voltage at node "S_{out}" is < $V_{dd}/2$, the n-CNTFET (T_7) in the level restorer is turned OFF, the p-CNTFET (Q_3) is always in ON condition irrespective of the applied input; then the output of inverter becomes logic '0'. The output of the T_7 and Q_3 CNTFETs is logic '0', it is applied to the input of pull-up p-CNTFET (Q_2), then the pull-up p-CNTFET (Q_2) is turned ON, and the node "S_{out}" is charged with an effective drive current that equals the current of the n-CNTFET network.

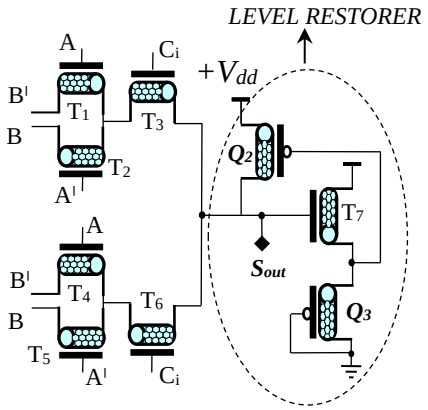


Figure. 4: CNTFET based proposed full adder sum circuit level restorer structure-II (within the dashed circle).

When the voltage at node "S_{out}" reaches to $V_{dd}/2$, the n-CNTFET (T_7) in the level restorer is turned ON, then the p-CNTFET (Q_3) is always in ON condition irrespective of its applied input; then the output of inverter is logic '1'. The output of the T_7 and Q_3 CNTFETs is logic '1', it is applied to the input of pull-up p-CNTFET (Q_2), then the pull-up p-CNTFET (Q_2) is turned OFF, and the node "S_{out}" is charged with an effective drive current that equals the current of the n-CNTFET network. The carry circuit shown in Fig 3(b) is the same for both of the proposed full adders. In carry circuit complimentary logic is used where it can be classified as N-CNTFETs and P-CNTFETs. It is composed of branch based logic where all the transistors are connected in series. Finally, the expression can be obtained by using the k-maps.

$$Sum = A \oplus B \oplus C_{in} \quad (5)$$

$$Carry = A.B + C_{in}.(A + B) \quad (6)$$

3. Simulation Results

The proposed 1-BIT CNTFET based full adders with modified level restorers are simulated by using Spectre Cadence with 32 nm CNTFET technology files [28]. The circuits simulated on Cadence tool have been carried out with supply voltage V_{dd}= +0.8 V and frequency of f = 100 MHz. The design parameters and chirality values of Fig. 3 and Fig. 4 CNTFETS are shown in the Table. 1 below.

Table 1: 32 nm Stanford Model Technology Parameters.

Chiralities of Fig. 3 and Fig. 4

S.No	CNTFETS	Chiralities
1.	Q_1, Q_2, Q_3	(11, 0)
2.	$T_1 - T_{22}$	(19, 0)
3.	Physical Channel Length	32 nm
4.	Oxide thickness	4 nm
5.	Dielectric Constatnt	16
6.	Power Supply	0.8 V
7.	Threshold Voltage	0.49

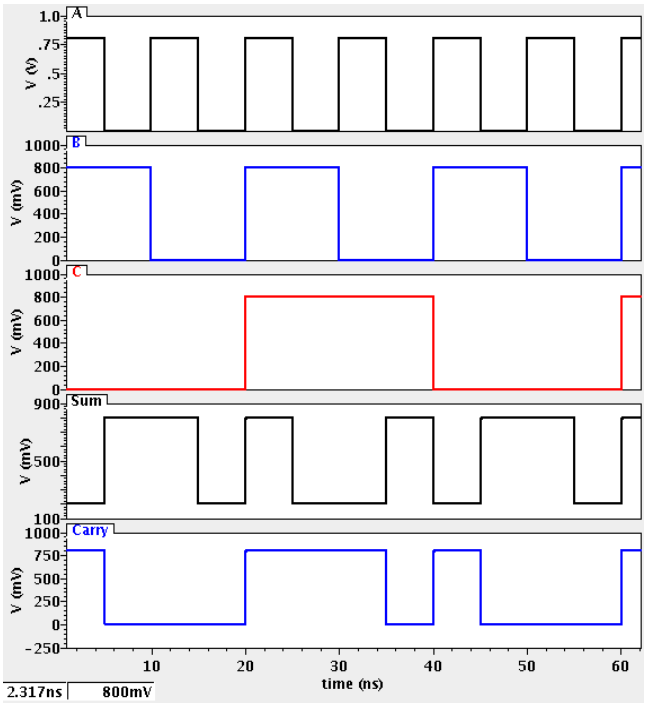


Figure. 5: Simulated input & output waveforms of full adder with level restorer structure-I of Fig. 3.

The simulated input and output waveforms of the proposed adders Fig. 3 and 4 are shown as above in Fig. 5 and Fig. 6. The simulated total power consumption of Fig. 3 is 0.1395 µw and Fig. 4 is 0.142 µW.

In the BBL-PT full adder, there existed a voltage step in the sum output waveform during 0 → 1 transition [1] and the same was eliminated in the T.V. Rao *et. al* proposed full adder designs using current sink inverter and current source inverter with the supply rail voltage of +1.2 V [2]. The voltage step in BBL-PT is due to the delay needed by the level restorer to restore the weak logic '1' level. The proposed level restorers shown in Fig. 3(a) and Fig. 4 does not require delay to restore the weak logic '1' level. In Fig. 3 and 4, the inputs (A, B & C) applied for all possible combinations i.e. 000 to 111.

In the Table. 2 shown as under the candidate's design has been compared with the supply voltages and the proposed circuits also proved consuming less power.

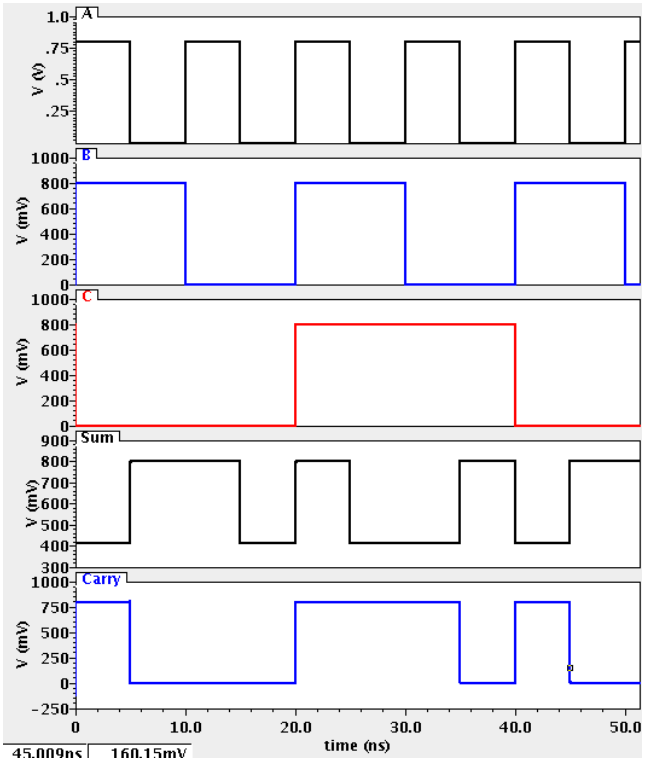


Figure. 6. Simulated input & output waveforms of full adder with level restorer structure-II of Fig. 4.

Table 2: Comparison of earlier published full adder circuits with supply rail voltage

Reference number	Type of transistors used	Supply voltage (V)
I. Hassoune *et. al* [1]	MOSFETs	+1.2
T. V. Rao *et. al* [2]	MOSFETs	+1.2

D.Radhakrishnan [3]	MOSFETs	+3
D. Datta *et. al* [4]	MOSFETs	+2.5
Y. S. Mehrabani *et. al* [5]	CNTFETs	+0.9
S. R. Prasad *et. al* [6]	CNTFETs	+0.9
Proposed circuits Fig. 3(a) and 4	CNTFETs	+0.8

5. Conclusion

In this paper, two CNTFET based BBL-PT full adders with level restorers are presented. Two new circuits decrease the existing diffusion capacitances and also eliminate the voltage step. The designed full adder circuits attain less power consumption when compared to the traditional MOSFET. Hence, these circuits can be implemented in many applications such as ripple carry adder, multipliers, ALUs etc.

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